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(54) **ORGANIC LIGHT-EMITTING DIODE DISPLAY**

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(57) **ABSTRACT**

An organic light-emitting diode (OLED) display is disclosed. In one aspect, the OLED display includes a substrate including a display area in which an OLED is formed and a non-display area surrounding the display area. The OLED display also includes a pixel defining layer formed over the substrate and having an opening defining an emission area of the OLED, a first passivation layer covering a portion of the pixel defining layer formed in the non-display area and a second passivation layer formed in the non-display area, wherein a portion of the second passivation layer does not overlap the first passivation layer in the depth dimension of the OLED display. The OLED display further includes an encapsulation substrate formed to be opposite to the substrate and a filler filling a space between the substrate and the encapsulation substrate and contacting the first and second passivation layers.

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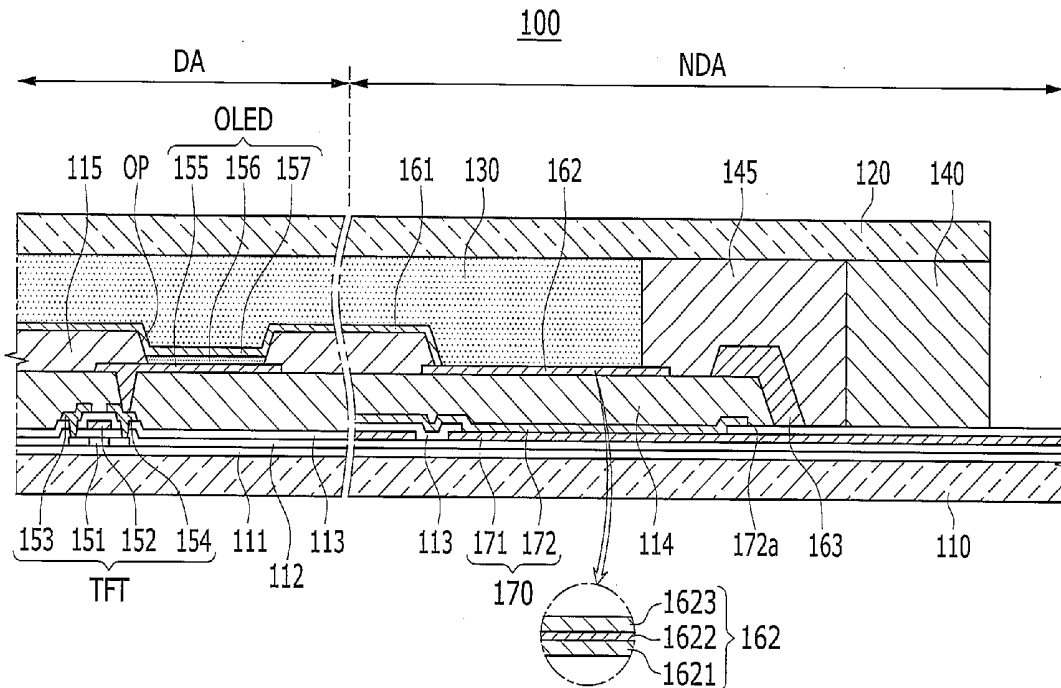


FIG. 1

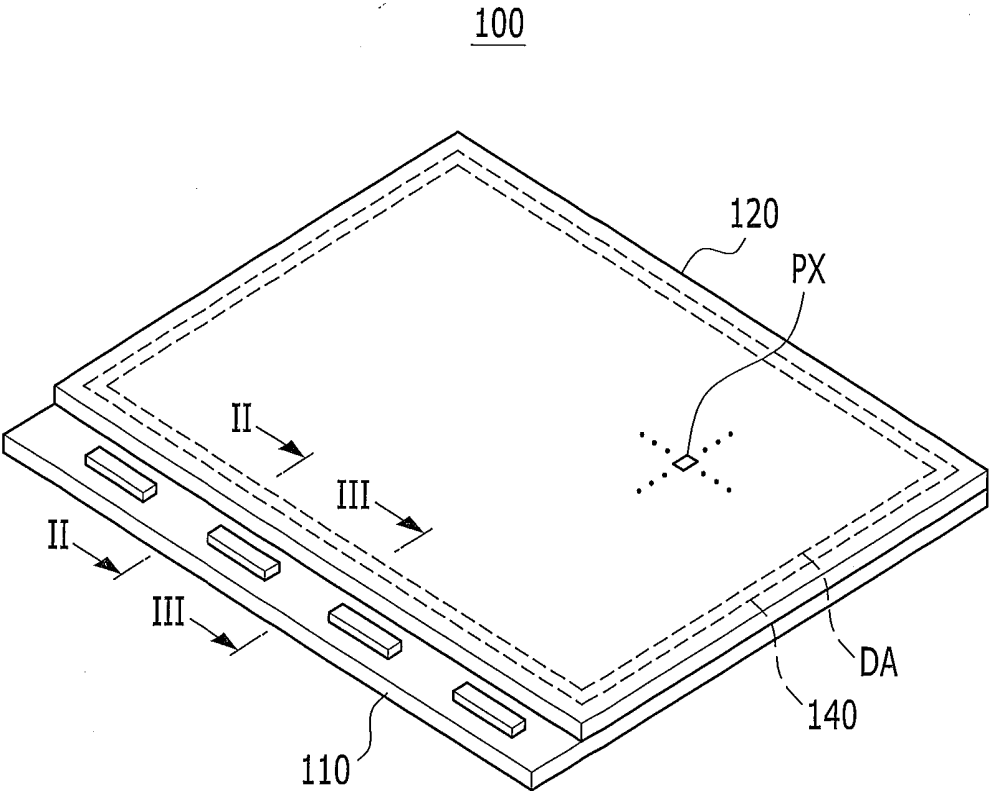


FIG. 3

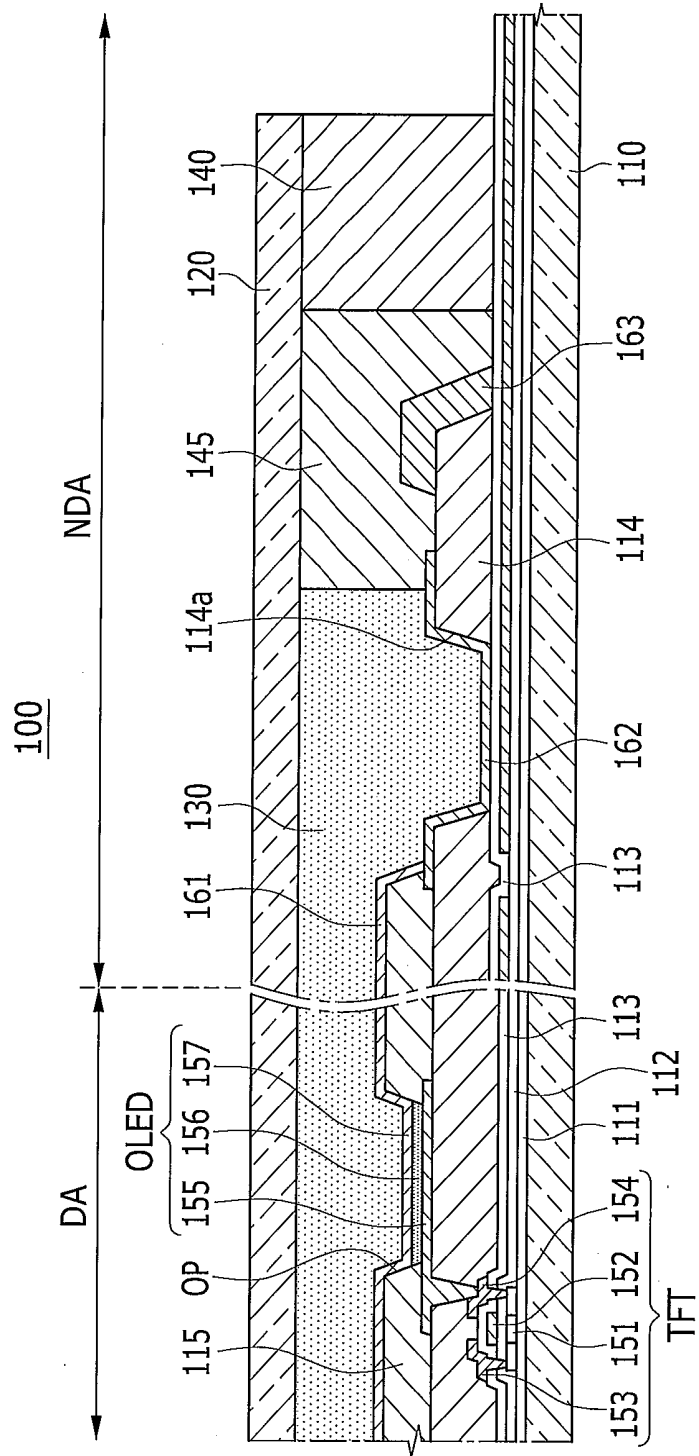


FIG. 4

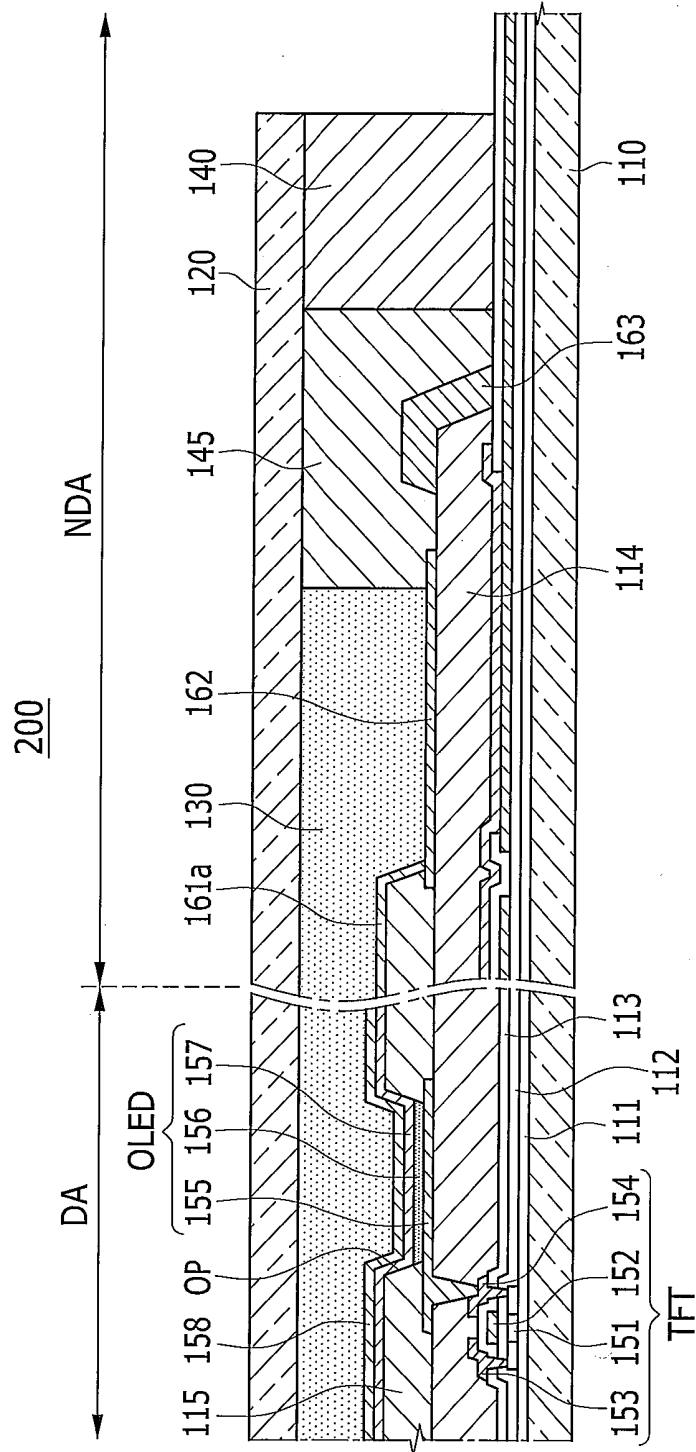
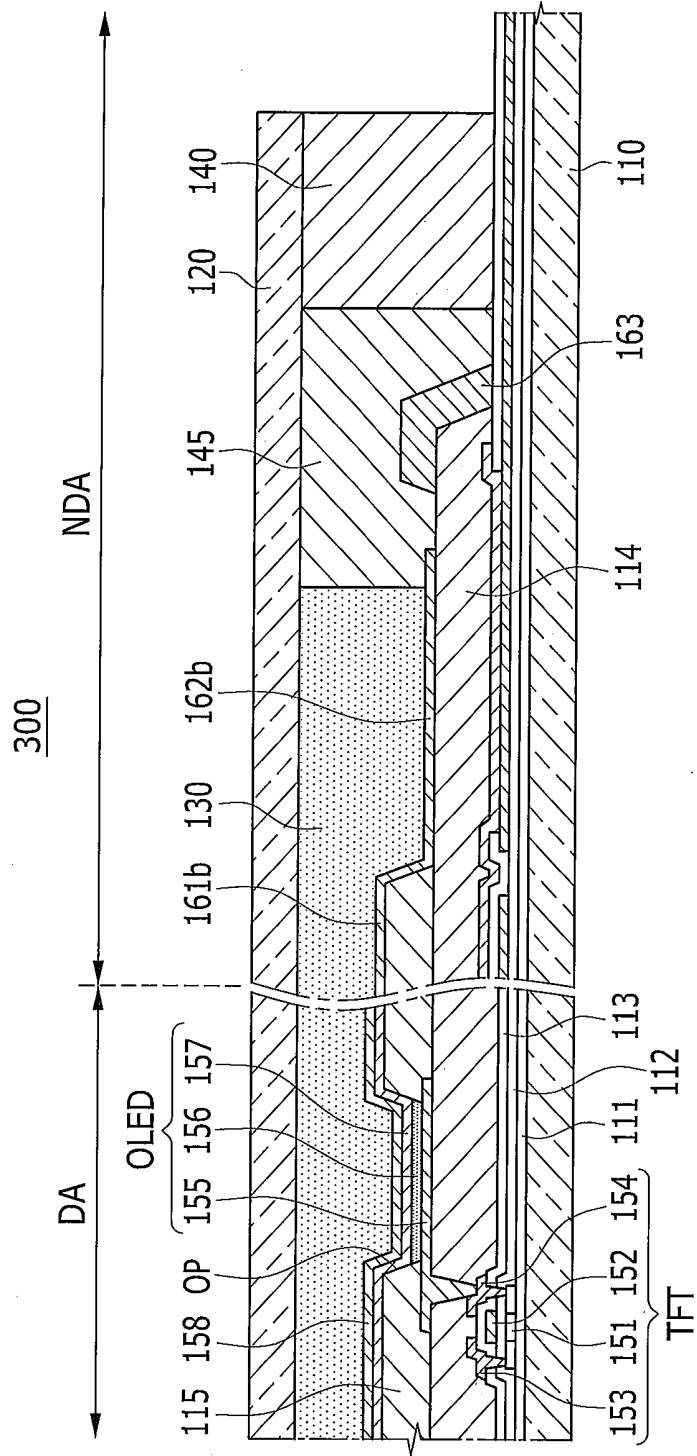


FIG. 5



ORGANIC LIGHT-EMITTING DIODE DISPLAY

RELATED APPLICATIONS

[0001] This application claims priority to and the benefit of Korean Patent Application No. 10-2015-0052481 filed in the Korean Intellectual Property Office on Apr. 14, 2015, the entire contents of which are incorporated herein by reference.

BACKGROUND

[0002] 1. Field

[0003] The described technology generally relates to an organic light-emitting diode display.

[0004] 2. Description of the Related Technology

[0005] An organic light emitting diode (OLED) display does not need a separate light source and therefore may have reduced thickness and weight. In addition, OLED displays have favorable characteristics such as low power consumption, high luminance, and a high reaction speed.

[0006] A typical OLED display includes a substrate, a driving circuit unit formed and an OLED, which are formed on the substrate, a pixel defining layer which defines an emission area of the OLED, and an encapsulation substrate formed to be opposite to the substrate. The substrate and the encapsulation substrate are integrally bonded to each other by a sealant and a space between the substrate and the encapsulation substrate may be filled with a filler. The filler serves to increase stiffness of the OLED display so as to enhance durability.

[0007] The above information disclosed in this Background section is only for enhancement of understanding of the background of the described technology and therefore it may contain information that does not form the prior art that is already known in this country to a person of ordinary skill in the art.

SUMMARY OF CERTAIN INVENTIVE ASPECTS

[0008] One inventive aspect relates to an OLED display that can prevent defects, such as a pixel contraction, due to a filler.

[0009] Another aspect is an OLED display that can suppress the occurrence of defects such as pixel contraction by blocking various impurities, oxygen, or the like, included in a filler from permeating into an OLED through a pixel defining layer and a planarization layer.

[0010] Another aspect is an OLED display including: a substrate including a display area in which an OLED is formed and a non-display area outside the display area; a pixel defining layer formed on the substrate and including an opening defining an emission area of the OLED; a first passivation layer covering a surface of a portion formed in the non-display area, in the pixel defining layer; a second passivation layer formed outside the pixel defining layer in the non-display area; an encapsulation substrate formed to be opposite to the substrate; and a filler filling a space between the substrate and the encapsulation substrate and contacting the first passivation layer and the second passivation layer.

[0011] An end of the pixel defining layer may be positioned between an edge of the display area and an edge of

the filler on a plane. The second passivation layer may contact the first passivation layer.

[0012] The OLED display may further include: a planarization layer formed under the pixel defining layer and the second passivation layer. The second passivation layer may cover the entire surface of the planarization layer outside the pixel defining layer. The pixel defining layer and the passivation layer may include silicon-based polymer.

[0013] The planarization layer may form an opening to expose an interlayer insulating layer under the planarization layer and the second passivation layer may cover the exposed interlayer insulating layer.

[0014] The OLED may include a pixel electrode, an emission layer, and a common electrode and may be covered with a capping layer. The first passivation layer may contact the common electrode and may be made of the same material as the common electrode. The second passivation layer may contact the first passivation layer and may be made of the same material as the pixel electrode.

[0015] The first passivation layer may contact the capping layer and may be made of the same material as the capping layer. The second passivation layer may contact the first passivation layer and may be made of the same material as the pixel electrode. The second passivation layer may be formed of a multilayer of a first transparent layer, a metal thin layer and a second transparent layer.

[0016] The first passivation layer may contact the capping layer and may be made of the same material as the capping layer and the second passivation layer may contact the first passivation layer and may be made of the same material as the capping layer.

[0017] Another aspect is an organic light-emitting diode (OLED) display, including: a substrate including a display area in which an OLED is formed and a non-display area surrounding the display area; a pixel defining layer formed over the substrate and having an opening defining an emission area of the OLED; a first passivation layer covering a portion of the pixel defining layer formed in the non-display area; a second passivation layer formed in the non-display area, wherein a portion of the second passivation layer does not overlap the first passivation layer in the depth dimension of the OLED display; an encapsulation substrate formed to be opposite to the substrate; and a filler filling a space between the substrate and the encapsulation substrate and contacting the first and second passivation layers.

[0018] In the above OLED display, an end of the pixel defining layer is positioned between an edge of the display area and an edge of the filler on a plane. In the above OLED display, the second passivation layer contacts the first passivation layer. The above OLED display further comprises: a planarization layer formed below the pixel defining layer and the second passivation layer, wherein the second passivation layer covers substantially the entire surface of the planarization layer outside the pixel defining layer. In the above OLED display, each of the pixel defining layer and the passivation layer is formed of silicon-based polymer. In the above OLED display, the planarization layer forms an opening to expose an interlayer insulating layer formed below the planarization layer and wherein the second passivation layer covers the exposed interlayer insulating layer.

[0019] In the above OLED display, the OLED includes a pixel electrode, an emission layer, and a common electrode and is covered with a capping layer. In the above OLED display, the first passivation layer contacts the common

electrode and is formed of the same material as the common electrode. In the above OLED display, the second passivation layer contacts the first passivation layer and is formed of the same material as the pixel electrode. In the above OLED display, the first passivation layer contacts the capping layer and is formed of the same material as the capping layer. In the above OLED display, the second passivation layer contacts the first passivation layer and is formed of the same material as the pixel electrode. In the above OLED display, the second passivation layer is formed of a multilayer of a first transparent layer, a metal thin layer, and a second transparent layer.

[0020] In the above OLED display, the second passivation layer is formed of a multilayer of a first transparent layer, a metal thin layer, and second transparent layer. In the above OLED display, the first passivation layer contacts the capping layer and wherein the second passivation layer contacts the first passivation layer and is formed of the same material as the capping layer. In the above OLED display, the first and second passivation layers are formed on different layers. In the above OLED display, the first passivation layer is formed above the second passivation layer.

[0021] Another aspect is an organic light-emitting diode (OLED) display, including: an OLED formed in a display area; a pixel defining layer including a first portion formed in the display area and a second portion formed in a non-display area surrounding the display area; a first passivation layer covering at least the second portion of the pixel defining layer; a second passivation layer formed in the non-display area, wherein the second passivation layer contacts a portion of the first passivation layer and part of the second portion of the pixel defining layer; and a filler covering the first and second passivation layers.

[0022] In the above OLED display, the second passivation layer includes a portion that does not overlap the first passivation layer in the depth dimension of the OLED display. In the above OLED display, the first passivation layer includes a non-linear portion, and wherein the second passivation layer is substantially linear. In the above OLED display, the first and second passivation layers are formed on different layers.

[0023] According to at least one of the disclosed embodiments, it is possible to prevent various impurities, oxygen, and the like which are included in the filler from diffusing into the pixel defining layer and the planarization layer by allowing the first and second passivation layers to block the contact between the pixel defining layer and the planarization layer and the filler. It is possible to suppress the defects, such as the deterioration in the OLED and the pixel contraction, due to the filler.

BRIEF DESCRIPTION OF THE DRAWINGS

[0024] FIG. 1 is a perspective view of an OLED display according to a first exemplary embodiment.

[0025] FIG. 2 is a partially enlarged cross-sectional view of the OLED display taken along the line II-II of FIG. 1.

[0026] FIG. 3 is a partially enlarged cross-sectional view of the OLED display taken along the line of FIG. 1.

[0027] FIG. 4 is an enlarged cross-sectional view of an OLED display according to a second exemplary embodiment.

[0028] FIG. 5 is an enlarged cross-sectional view of an OLED display according to a third exemplary embodiment.

DETAILED DESCRIPTION OF CERTAIN INVENTIVE EMBODIMENTS

[0029] Hereinafter, the present disclosure will be described more fully hereinafter with reference to the accompanying drawings, in which exemplary embodiments of the disclosure are shown. As those skilled in the art would realize, the described embodiments may be modified in various different ways, all without departing from the spirit or scope of the present disclosure.

[0030] Throughout the present specification, it will be understood that when an element such as a layer, a film, a region, or a substrate is referred to as being “on” another element, it can be directly on the other element or intervening elements may also be present. Further, in the specification, the word “on” means positioning on or below the object portion, but does not essentially mean positioning on the upper side of the object portion based on a gravity direction.

[0031] In addition, unless explicitly described to the contrary, the word “comprise” and variations such as “comprises” or “comprising”, will be understood to imply the inclusion of stated elements but not the exclusion of any other elements. In addition, the size and thickness of each configuration shown in the drawings are arbitrarily shown for understanding and ease of description, but the present disclosure is not limited thereto. In this disclosure, the term “substantially” includes the meanings of completely, almost completely or to any significant degree under some applications and in accordance with those skilled in the art. The term “connected” can include an electrical connection.

[0032] FIG. 1 is a perspective view of an OLED display **100** according to a first exemplary embodiment and FIG. 2 is a partially enlarged cross-sectional view of the OLED display taken along the line II-II of FIG. 1.

[0033] Referring to FIG. 1, the OLED display **100** includes a substrate **110** including a display area DA and a non-display area NDA, a plurality of pixels PXs formed in the display area DA on the substrate **110**, an encapsulation substrate **120** formed to be opposite to the substrate **110**, and a filler **130** filling a space between the substrate **110** and the encapsulation substrate **120**. The substrate **110** and the encapsulation substrate **120** are bonded to each other to be integrally sealed with a sealant **140**.

[0034] In the display area DA, an image is displayed by a combination of light emitted from the pixels PXs. Each pixel PX includes a driving circuit unit or driving circuit and an OLED. The driving circuit unit includes at least two thin film transistors and at least one capacitor. A pixel defining layer **115** which defines an emission area of the OLED is formed on the substrate **110**. The pixel defining layer **115** can be larger than the display area DA.

[0035] The OLED display **100** includes a first passivation layer **161** covering a surface of the pixel defining layer **115** in the non-display area NDA and a second passivation layer **162** contacting the first passivation layer **161** and formed outside the pixel defining layer **115**. The filler **130** contacts the first passivation layer **161** and the second passivation layer **162** in the non-display area NDA.

[0036] The first and second passivation layers **161** and **162** block the pixel defining layer **115** and the planarization layer **114** from contacting the filler **130** to prevent various impurities or oxygen included in the filler **130** from diffusing into the pixel defining layer **115** and the planarization layer **114**.

Therefore, it is possible to suppress the defects, such as the deterioration in the OLED and the pixel contraction, due to the filler 130.

[0037] Hereinafter, a cross section structure of the OLED display 100 will be described in more detail.

[0038] A buffer layer 111 is formed on the substrate 110. The substrate 110 may be formed of glass, quartz, ceramic, polymer film, and the like and may have light transparency. The buffer layer 111 may have a single layer which is made of silicon nitride (SiN_x) or a double layer which is made of silicon nitride (SiN_x) and silicon oxide SiO₂. The buffer layer 111 serves to planarize a surface while preventing permeation of impurities through the substrate 110.

[0039] A semiconductor layer 151 may be formed on the buffer layer 111. The semiconductor layer 151 may be made of a polysilicon or an oxide semiconductor and the semiconductor layer 151 which is made of the oxide semiconductor may be covered with a separate passivation layer. The semiconductor layer 151 includes a channel region which is not doped with impurity and a source region and a drain region which are positioned at both sides of the channel region and are doped with impurity.

[0040] A gate insulating layer 112 is formed on the semiconductor layer 151. The gate insulating layer 112 may be formed of a single layer of silicon nitride (SiN_x) or silicon oxide SiO₂ or a stacked layer thereof. A gate electrode 152 is formed on the gate insulating layer 112. The gate electrode 152 overlaps the channel region of the semiconductor layer 151 and may include Au, Ag, Cu, Ni, Pt, Pd, Al, Mo, and the like.

[0041] An interlayer insulating layer 113 is formed on the gate electrode 152. The interlayer insulating layer 113 may be formed of a single layer of silicon nitride (SiN_x) or silicon oxide SiO₂ or a stacked layer thereof.

[0042] A source electrode 153 and a drain electrode 154 are formed on the interlayer insulating layer 113. The source electrode 153 and the drain electrode 154 are each connected to the source region and the drain region of the semiconductor layer 151 through the via holes which are formed on the interlayer insulating layer 113 and the gate insulating layer 112. The source electrode 153 and the drain electrode 154 may be formed of a metal multilayer film such as Mo/Al/Mo and Ti/Al/Ti.

[0043] FIG. 2 illustrates, for example, the driving thin film transistor (TFT) of a top gate type, but the structure of the driving thin film transistor (TFT) is not limited to the illustrated example. The driving circuit unit includes a switching thin film transistor, a driving thin film transistor, and a storage capacitor and for convenience, FIG. 2 illustrates only the driving thin film transistor (TFT).

[0044] The driving thin film transistor (TFT) is covered with a planarization layer 114 and is connected to the OLED to drive the OLED. A pixel electrode 155 is formed on the planarization layer 114. The pixel electrode 155 is formed in each pixel one by one and is connected to the drain electrode 154 of the driving thin film transistor (TFT) via the via holes which are formed on the planarization layer 114.

[0045] The pixel defining layer 115 is formed on the planarization layer 114 and the pixel electrode 155. The pixel defining layer 115 forms an opening OP to expose a central portion of the pixel electrode 155 on which the emission layer 156 will be positioned. That is, the opening OP serves to define the emission area of the OLED.

[0046] The pixel defining layer 115 may be made of relatively inexpensive silicon-based polymer which replaces expensive photosensitive polyimide. Further, the planarization layer 114 may also be made of the same silicon-based polymer as the pixel defining layer 115. This reduces the cost of materials which contributes in reducing the costs of the OLED display 100.

[0047] The emission layer 156 is formed on the pixel electrode 155 and the common electrode 156 is formed on the emission layer 156 and the pixel defining layer 115. The common electrode 157 is formed in the whole display area (DA) without being differentiated for each pixel. Any one of the pixel electrode 155 and the common electrode 157 injects holes into the emission layer 156 and the other thereof injects electrons into the emission layer 156.

[0048] The emission layer 156 includes an organic emission layer and includes at least one of a hole injection layer, a hole transportation layer, an electron transportation layer, and an electron injection layer. When the pixel electrode 155 is an anode injecting holes, a hole injection layer, a hole transport layer, an organic emission layer, an electron transport layer, and an electron injection layer may be sequentially stacked on the pixel electrode 155. The rest of the layers other than the organic emission layer may be formed over the whole of the display area DA.

[0049] When the OLED display 100 is a bottom emission type, the pixel electrode 155 is formed of the transparent layer or the translucent layer and the common electrode 157 is formed of the reflecting layer. The light emitted from the emission layer 156 is reflected from the common electrode 157 and transmits the pixel electrode 155 and the substrate 110 to be emitted to the outside. When the pixel electrode 155 is formed of the translucent layer, a portion of the light emitted from the common electrode 157 is again reflected from the pixel electrode 155, and the pixel electrode 155 and the common electrode 157 form a resonance structure to increase light extraction efficiency.

[0050] When the OLED display 100 is a top emission type, the pixel electrode 155 is formed of a reflecting layer and the common electrode 157 is formed of a transparent layer or a translucent layer.

[0051] The reflecting layer may include Au, Ag, Mg, Al, Pt, Pd, Ni, Nd, Ir, Cr, and the like. The transparent layer may include indium tin oxide (ITO), indium zinc oxide (IZO), ZnO, In₂O₃, and the like. The translucent layer may be formed of a metal thin layer including Li, Ca, LiF/Ca, LiF/Al, Al, Ag, Mg, and the like and may be formed of a stacked layer of the metal thin layer and the transparent layer. For example, the translucent layer may be formed of a multilayer of ITO/Ag/ITO.

[0052] The substrate 110 and the encapsulation substrate 120 are bonded to each other by a sealant 140. The sealant 140 is formed at edges of the substrate 110 and the encapsulation substrate 120 and may include inorganic materials such as glass frit or organic materials such as epoxy. Inside of the sealant may be formed with a getter 145. The getter 145 serves to adsorb moisture or oxygen permeated through the sealant 140 and may include CaO, BaO, MgO, and the like having excellent reactivity with moisture or oxygen.

[0053] A space between the substrate 110 and the encapsulation substrate 120 inside of the getter 145 is filled with the filler 130. The filler 130 fills an empty space between the substrate 110 and the encapsulation substrate 120 to serve to increase stiffness of the OLED display 100. That is, the

OLED display 100 including the filler 130 has improved durability against external impact, for example, dropping. The filler 130 may be a transparent isotropic material and may include transparent silicon-based polymer.

[0054] The buffer layer 111, the gate insulating layer 112, and the interlayer insulating layer 113 may be formed as the same size as the substrate 110 and the planarization layer 114 may be formed to be smaller than the interlayer insulating layer 113 so that the edge of the planarization layer overlaps the getter 145 on the plane. Further, an end of the pixel defining layer 115 may be positioned between the edge of the display area DA and the edge of the filler 130 on the plane. The edge of the pixel defining layer 115 is spaced apart from the getter 145 at a predetermined distance.

[0055] In the pixel defining layer 115, the surface of the portion formed in the display area DA is covered with the common electrode 157 and the surface of the portion formed in the non-display area NDA is covered with the first passivation layer 161. The first passivation layer 161 covers both an upper surface and a side of the pixel defining layer 115. Further, the second passivation layer 162 contacts the first passivation layer 161 and is formed outside the pixel defining layer 115.

[0056] Both of the first passivation layer 161 and the second passivation layer 162 are formed in the non-display area NDA and may include metal, an inorganic material, or an organic material into which the material of the filler 130 is not diffused.

[0057] The first passivation layer 161 may be made of the same material as the common electrode 157. The first passivation layer 161 may be integrally formed with the common electrode 157, while contacting the common electrode 157. For example, the common electrode 157 and the first passivation layer 161 may be simultaneously formed by enlarging an opening size of an open mask used at the time of depositing the common electrode 157.

[0058] The second passivation layer 162 is formed between the planarization layer 114 and the filler 130, outside of the pixel defining layer 115. Both ends of the second passivation layer 162 may overlap the pixel defining layer 115 and the getter 145. That is, the second passivation layer 162 may include one end overlapping the pixel defining layer 115, a central portion overlapping the filler 130, and the other end overlapping the getter 145.

[0059] The second passivation layer 162 may be made of the same material as the pixel electrode 155 and may be simultaneously formed with the pixel electrode 155. For example, the common electrode 155 and the second passivation layer 162 may be simultaneously formed by adding the opening size to a deposition mask used at the time of depositing the common electrode 155. Therefore, a separate deposition mask for forming the second passivation layer 162 is not required and a manufacturing process for forming the second passivation layer 162 is not added.

[0060] When the pixel electrode 155 is formed of the translucent layer, the second passivation layer 162 may be formed of a multilayer of a first transparent layer 1621, a metal thin layer 1622, and a second transparent layer 1623, for example, a multilayer of ITO/Ag/ITO. The first transparent layer 1621 has excellent adhesion with the planarization layer 114 and the second transparent layer 1623 has excellent adhesion with the filler 130. Therefore, the second passivation layer 162 may be firmly formed between the

planarization layer 114 and the filler 130 without defects such as lifting and delamination.

[0061] By the foregoing configuration, the filler 130 contacts the first and second passivation layers 161 and 162 in the non-display area NDA and does not contact the pixel defining layer 115 and the planarization layer 114. The pixel defining layer 115, the planarization layer 114, and the filler 130 all may be made of silicon-based polymer and when the filler 130 contacts the pixel defining layer 115 and the planarization layer 114 including the same-based polymer, the material is easily diffused.

[0062] For example, if it is assumed that the pixel defining layer 115 is formed to be wider than the filler 130 to contact the getter 145, the surface of the pixel defining layer 115 which is not covered with the common electrode 157 in the non-display area NDA contacts the filler 130. Further, if it is assumed that no second passivation layer 162 is present in the structure of FIG. 2, the filler 130 contacts the planarization layer 114.

[0063] In this case, various impurities, oxygen, or the like which is included in the filler 130 is easily diffused into the pixel defining layer 115 and the planarization layer 114. Further, the impurities or the oxygen which is diffused into the pixel defining layer 115 and the planarization layer 114 is permeated into the OLED to cause the deterioration in the OLED and defects such as pixel contraction.

[0064] However, according to some embodiments, the pixel defining layer 115 and the planarization layer 114 do not contact the filler 130 by the first passivation layer 161 and the second passivation layer 162 and therefore the diffusion of the material from the filler 130 into the pixel defining layer 115 and the planarization layer 114 may be prevented. Therefore, according to the OLED display 100 according to the first exemplary embodiment, it is possible to suppress defects, such as the deterioration in the OLED and the pixel contraction, due to the filler 130.

[0065] Meanwhile, a wiring 170 for supplying an electrical signal to the pixels PXs may be positioned in the non-display area NDA. The wiring 170 may include a first metal layer 171 formed on the gate insulating layer 112 and a second metal layer 172 contacting the first metal layer 171 by the opening formed on the interlayer insulating layer 113. The first metal layer 171 may be made of the same material as the gate electrode 152 and the second metal layer 172 may be made of the same material as the source electrode 153 and drain electrode 154.

[0066] The second metal layer 172 may include an end 172a protruding from the insulating layer 113 in the area overlapping the getter 145

[0067] The third passivation layer 163 may be formed on the edge of the planarization layer 114 into the getter 114. The third passivation layer 163 prevents the defects such as lifting or delamination of the second metal layer 172 and the planarization layer 114 due to the protruding end 172a of the second metal layer 172. The third passivation layer 163 may be made of the same material as the pixel defining layer 115, simultaneously formed with the pixel defining layer 115.

[0068] FIG. 3 is a partially enlarged cross-sectional view of the OLED display taken along the line of FIG. 1.

[0069] Referring to FIG. 3, the opening 114a may be formed on the planarization layer 114, if necessary, in the portion which does not overlap the wiring in the non-display area NDA. The surface of the interlayer insulating layer 113 is exposed by the opening 114a of the planarization layer

114 and the second passivation layer **162** is formed on the side wall of the planarization layer **114** enclosing the opening **114a** and over the exposed interlayer insulating layer **113**.

[0070] The second passivation layer **162** made of the same material as the pixel electrode **155** has excellent adhesion with the interlayer insulating layer **113** and the filler **130**. Therefore, it is possible to suppress defects such as lifting or delamination of the interlayer insulating layer **113** exposed by the opening **114a** of the planarization layer **114**.

[0071] FIG. 4 is an enlarged cross-sectional view of an OLED display **200** according to a second exemplary embodiment.

[0072] Referring to FIG. 4, the OLED display **200** includes a capping layer **158** formed on the common electrode **157** and is made of the same material as a first passivation layer **161a** and the capping layer **158**. The first passivation layer **161a** may be integrally formed with the capping layer **158**, while contacting the capping layer **158**.

[0073] The capping layer **158** protects the OLED display and when the OLED display **200** is the top emission type, serves to optimize the light efficiency by refractive index matching. The capping layer **158** may include organic materials such as Alq₃(tris (8-hydroxyquinoline) aluminum), α -NPD(N,N'-bis-(naphthalene-1-yl)-N,N'-bis(phenyl)benzidine), NPB(N,N'-Bis-(1-naphthyl)-N,N-Diphenyl-1,1-Biphenyl-4-4'-Diamine), or CuPc(Copper Phthalocyanine).

[0074] The rest of the components other than the capping layer **158** and the first passivation layer **161a** are the same as the first exemplary embodiment as described above.

[0075] FIG. 5 is an enlarged cross-sectional view of an OLED display **300** according to a third exemplary embodiment.

[0076] Referring to FIG. 5, the OLED display **300** includes the capping layer **158** formed on the common electrode **157** and a first passivation layer **161b** and a second passivation layer **162b** are made of the same material as the capping layer **158**. The first passivation layer **161b** may be integrally formed with the capping layer **158** while contacting the capping layer **158** and the second passivation layer **162b** may be integrally formed with the first passivation layer **161b** while contacting the first passivation layer **161b**. That is, the capping layer **158**, the first passivation layer **161b**, and the second passivation layer **162b** may be formed of a single layer.

[0077] The rest of the components other than the capping layer **158**, the first passivation layer **161b**, and the second passivation layer **162b** are the same as the first exemplary embodiment as described above.

[0078] While the inventive technology has been described in connection with exemplary embodiments, it is to be understood that the invention is not limited to the disclosed embodiments, but, on the contrary, is intended to cover various modifications and equivalent arrangements included within the spirit and scope of the appended claims.

What is claimed is:

1. An organic light-emitting diode (OLED) display, including:

a substrate including a display area in which an OLED is formed and a non-display area surrounding the display area;

a pixel defining layer formed over the substrate and having an opening defining an emission area of the OLED;

a first passivation layer covering a portion of the pixel defining layer formed in the non-display area;

a second passivation layer formed in the non-display area, wherein a portion of the second passivation layer does not overlap the first passivation layer in the depth dimension of the OLED display;

an encapsulation substrate formed to be opposite to the substrate; and

a filler filling a space between the substrate and the encapsulation substrate and contacting the first and second passivation layers.

2. The OLED display of claim 1, wherein an end of the pixel defining layer is positioned between an edge of the display area and an edge of the filler on a plane.

3. The OLED display of claim 2, wherein the second passivation layer contacts the first passivation layer.

4. The OLED display of claim 3, further comprising:

a planarization layer formed below the pixel defining layer and the second passivation layer, wherein the second passivation layer covers substantially the entire surface of the planarization layer outside the pixel defining layer.

5. The OLED display of claim 4, wherein each of the pixel defining layer and the passivation layer is formed of silicon-based polymer.

6. The OLED display of claim 4, wherein the planarization layer forms an opening to expose an interlayer insulating layer formed below the planarization layer and wherein the second passivation layer covers the exposed interlayer insulating layer.

7. The OLED display of claim 1, wherein the OLED includes a pixel electrode, an emission layer, and a common electrode and is covered with a capping layer.

8. The OLED display of claim 7, wherein the first passivation layer contacts the common electrode and is formed of the same material as the common electrode.

9. The OLED display of claim 8, wherein the second passivation layer contacts the first passivation layer and is formed of the same material as the pixel electrode.

10. The OLED display of claim 7, wherein the first passivation layer contacts the capping layer and is formed of the same material as the capping layer.

11. The OLED display of claim 10, wherein the second passivation layer contacts the first passivation layer and is formed of the same material as the pixel electrode.

12. The OLED display of claim 9, wherein the second passivation layer is formed of a multilayer of a first transparent layer, a metal thin layer, and a second transparent layer.

13. The OLED display of claim 11, wherein the second passivation layer is formed of a multilayer of a first transparent layer, a metal thin layer, and second transparent layer.

14. The OLED display of claim 7, wherein the first passivation layer contacts the capping layer and is formed of the same material as the capping layer and wherein the second passivation layer contacts the first passivation layer and is formed of the same material as the capping layer.

15. The OLED display of claim 1, wherein the first and second passivation layers are formed on different layers.

16. The OLED display of claim **1**, wherein the first passivation layer is formed above the second passivation layer.

17. An organic light-emitting diode (OLED) display, including:

an OLED formed in a display area;

a pixel defining layer including a first portion formed in the display area and a second portion formed in a non-display area surrounding the display area;

a first passivation layer covering at least the second portion of the pixel defining layer;

a second passivation layer formed in the non-display area, wherein the second passivation layer contacts a portion of the first passivation layer and part of the second portion of the pixel defining layer; and

a filler covering the first and second passivation layers.

18. The OLED display of claim **17**, wherein the second passivation layer includes a portion that does not overlap the first passivation layer in the depth dimension of the OLED display.

19. The OLED display of claim **17**, wherein the first passivation layer includes a non-linear portion, and wherein the second passivation layer is substantially linear.

20. The OLED display of claim **17**, wherein the first and second passivation layers are formed on different layers.

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专利名称(译)	有机发光二极管显示器		
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[标]申请(专利权)人(译)	三星显示有限公司		
申请(专利权)人(译)	三星DISPLAY CO. , LTD.		
当前申请(专利权)人(译)	三星DISPLAY CO. , LTD.		
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外部链接	Espacenet USPTO		

摘要(译)

公开了一种有机发光二极管 (OLED) 显示器。在一个方面, OLED显示器包括基板, 该基板包括其中形成有OLED的显示区域和覆盖该显示区域的非显示区域。 OLED显示器还包括形成在衬底上并具有限定OLED的发射区域的开口的像素限定层, 覆盖形成在非显示区域中的像素限定层的一部分的第一钝化层和形成在非显示区域中的第二钝化层在所述非显示区域中, 其中所述第二钝化层的一部分在所述OLED显示器的深度维度上不与所述第一钝化层重叠。 OLED显示器还包括形成为与基板相对的封装基板和填充在基板和位差封装基板之间的空间并且接触第一和第二钝化层的填充物。

